Implementation of Binary FFT Using Cordic Algorithm

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Abstract – The Fast Fourier transform (FFT) is one of the most significant algorithms in Digital Signal Processing.It is habituated to compute the Discrete Fourier Transform (DFT) efficiently. In order to enhance the high performance and real-time requirements of modern applications.This paper offer a new type of hardware architecture is called Binary FFT using specific rotation.The suggested architecture is based on the radix-2 FFT algorithm only half of the samples at each must be rotated.CORDIC algorithm habituated to reckon sine and cosine functions and a prototypical computer implementation. This algorithm is used to reckon rotation factor to deduce a figuring cost and area.Develop the binary version of FFT, in order to deduce processing overhead.This architecture has been coded in Verilog and simulated by using Xilinx software.

Index Terms – Commutator, Coordinate Rotation Digital Computer (CORDIC), Rotator, Processing element (PE).

1. INTRODUCTION

The Fast Fourier transform (FFT) is one of the most momentous algorithms in Digital Signal Processing.It is habituated to compute the Discrete Fourier Transform (DFT) efficaciously. In order to enhance the performance and real- time modern applications.The designers were tried to execute the efficacious architectures for the computation of the FFT. The pipelined architectures are widely evolved, because it furnish high throughput , low latency, low area and power consumption.It is suitable for some application such as Animation,Graphics,Image processing. There are two types of pipelined FFT. Serial pipelined & Parallel pipelined. Serial FFT,it enforce single instruction per clock cycle and Parallel FFT,it enforce several instruction per clock cycle. The FFT architectures are depicted by their loops, i.e., Feedforward or Feedback.In Feedback architectures, some outputs of the butterflies are fed back to the memories.It can be divided into Single path Delay Feedback (SDF)[2], which process a continuous flow of one sample per clock cycle, and Multipath Delay Feedback (MDF) [3], which process several samples in parallel.The feedforward architectures also known as Multi-path Delay Commutator (MDC) , it does not have feedback loops and each stage proceed the processed data to the next stage. The butterfly stages are habituated to get the output [1] .The hardware tools are reduced, hence the gate levels are optimized [5]. It habituates minimum amount of butterflies and memory by the use of rotator. The iterated values are stored in memory element[13]. It is a trade-off among butterflies, rotators and memoryThese architectures can also process several samples in parallel. In prevalent real- time employment, high interpretation requirements appear in anonymous applications such as Orthogonal Frequency Division Multiplexing (OFDM) and Ultra Wide Band (UWB).

2. RELATED WORKS

FFT is a way to evaluate Discrete Fourier transform result as more quickly.Fourier analysis is conversion of signal from time domain to frequency domain.It reduce the complexity of evaluating the DFT from $O(n^2)$ to $O(n \log n)$.The Cooley-tukey is a conquer algorithm that recursively breakdown a DFT. The N-point DFT of an input sequence x[n] is defined as,

$$X(k) = W_N^{kn} \quad (1)$$

$$W_N^{kn} = e^{-j2\pi kn/N} \quad (2)$$

$n = 0,1,2,3,.....N-1$

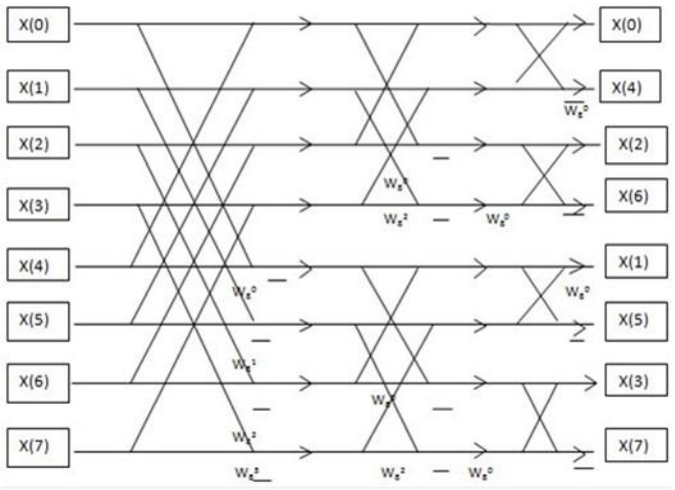

Figure 1.1 8 Point DIF FFT

There is two main expostulation can be distinguished. One is to calculate the FFT of multiple self-reliant data sequence. The FFT processors can participate the rotation recollection in order to demote the hardware. Second is to evaluate the FFT when several samples sequence are received in parallel. It is terminated to when the essential throughput is higher than the clock frequency of the device.It is essential to resort FFT architectures. CORDIC (Coordinate Rotation Digital Computer), is an arithmetic algorithm for efficicacious estimation of various transcend, Logarithmic, Exponential and trigonometric functions. It has been integrated in several arithmetic processors. Lately, it has been functioned to articulate and enforce in modern Digital Signal Processing (DSP) algorithms which require the estimation of sophisticated number multiplications, fundamental plane rotation.The Discrete Fourier Transform (DFT) is one of the most reckoning acute operation in Image compression.It has been used to Multimedia application.It is embraced in many standards such as JPEG, MPEG and H.264.

A disparate characteristic of the CORDIC algorithm habituates a sequence of fundamental rotations to realize a variety of sophisticated, nonlinear fundamental rotation require two simple shift-and-add operations to execute. It will reduces the latency (time between the attainable of input data and output), as well as hardware cost.

3. THE SERIAL COMMUTATOR OF FFT

The serial commutator (SC) FFT is based on the circuits for bit-dimension permutation of serial data.It habituates a novel data management.This Process is based on radix-2 FFT algorithm and only half of the samples at each stage must be rotated.

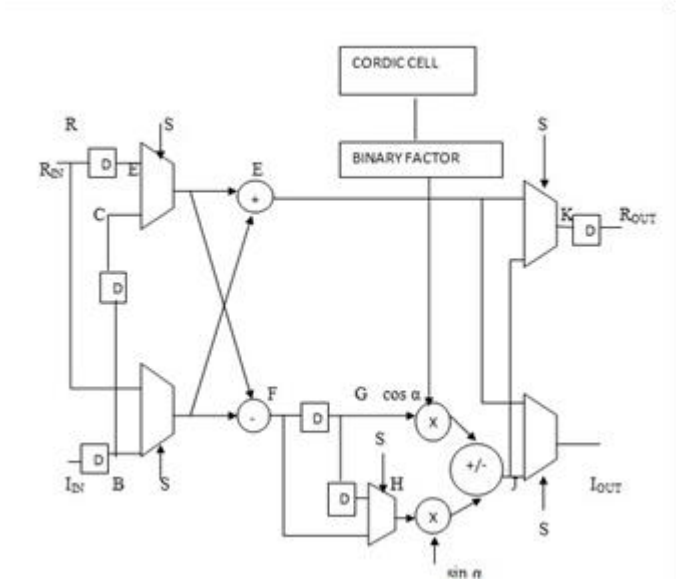

Figure 2.1 Processing Element of FFT

The processing element consist of butterfly and rotator. The radix-2 FFT architecture process one sample per clock cycle.It require only a complex adder and half a rotator per stage. The insignificant rotations are conveyed by rotators.The generic rotators are represented by a circle. Both butterflies and rotators are marked with N/2 . From that it require half of the components in butterflies and rotators.

A.Butterfly

The butterflies uses a real adder and real subtractor instead of complex arithmetic operation.By using the twiddle factor ,it evaluate the real and imaginary value of binary data.Twiddle factor values are varied fiom DIF and DIT.

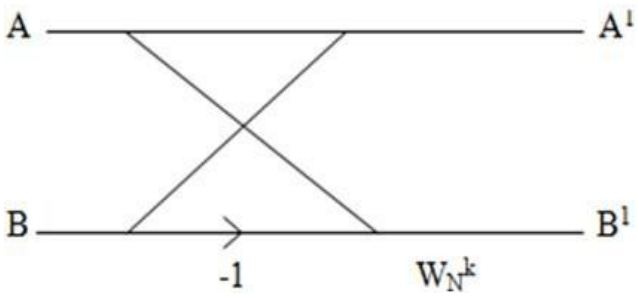

Figure 2.2 Twiddle Factor

$$W_N^k = e^{-j2\pi kn/N} \quad (3)$$

$$A^1 = A + B \quad (4)$$

$$B^1 = (A-B) * W_N^k \quad (5)$$

B.Rotator

The rotator is a term habituated to multiplexes the calculation in time.It require two real multipliers and one adder instead of four real multipliers and two adders. The half butterfly and half rotator form the processing element (PE) of the architecture.

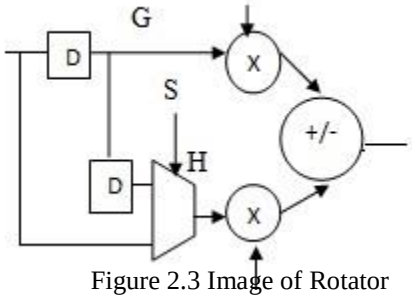

Figure 2.3 Image of Rotator

C. Data Management

The processing element evaluates a butterfly and a rotation on twain of data appear in sequential clock cycles.The data management of the SC FFT handled unperturbed in consecutive clock cycles. It transpire in all the stages of the FFT.

4. PROPOSED METHOD

It stands for (Co-ordinate Rotation Digital Computer) also known as Volder's algorithm.It converge one bit per iteration.Pseudo multiplication and pseudo division is used,when there is no hardware is available .It require only addition, subtraction, bit- shift and table look up. Sometimes it referred as Digital Resolver. The rotation-mode CORDIC algorithm is to rotate a vector [U_X ,U_Y] through an angle to is given by,

$$(U_X)i+1=(U_X)i-\sigma i(U_Y)i.2^{-i} \quad (6)$$

$$(U_Y)i+1=(U_Y)i+\sigma i(U_X)i.2^{-i} \quad (7)$$

$$\varphi i+1=\varphi i-\sigma i\tan^{-1}(2^{-i}) \quad (8)$$

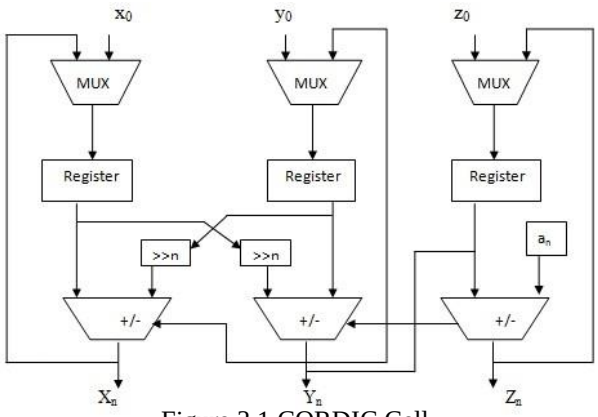

Figure 3.1 CORDIC Cell

It operates at two modes Rotation mode and Vectoring mode.In fixed rotation, it could be already executed and the sign-bits corresponding (φi) to might be stored in a sign-bit register (SBR) in CORDIC circuit [9]. The CORDIC circuit is not necessary evaluate to the remaining angle during the CORDIC iterations. CORDIC circuit for fixed rotations are corresponding to X and Y are fed as set/reset input to the twain of input registers and the successive feedback values X_I and Y_I at the iteration are fed in parallel to the input registers. The angle values are calculated using the CORDIC cell for required iteration.The angle values are fed to the Rotator through Binary factor for binary information. The data are processed and the output is received in R_{out} for real value and I_{out} for imaginary value. The conventional victual the pair of input registers with the initial values and as well as the feedback values are through a pair of multiplexers.

5. EXPERIMENTAL RESULT

The suggested fault compensation circuit with fixed width multiplier are simulated by using Xilinx ISE 12.1 and enforced in spartan-6 FPGA processor. During the execution, the parameters are taken from the synthesis report.The input is purely based on 0's and 1's. The experimental results are shown in table.

Table 1. Experimental result

s.no	Parameter	Existing	Proposed
1	SLICE	9	6
2	LUT	16	7
3	IOB	18	14

6. PERFORMANCE ANALYSIS

The interpretation of the suggested equatorial fault compensation with the subsisting scheme fixed width RPR are analyzed based on the area and fault compensation which was given below.The optimistic values are enforced better than the subsisting system. The proposed algorithm reduces area,power,look up table values and input output blocks.

7. SIMULATION RESULT

The simulation results are obtained from the Xilinx software.The coding are developed for the impementation of CORDIC, implementation of FFT and implementation of CORDIC with FFT.The synthesized reports are compared to the previous method.

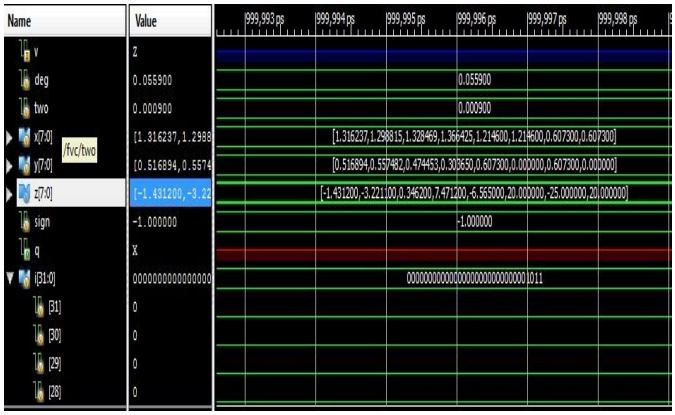

Figure 6.1 Output of CORDIC Algorithm

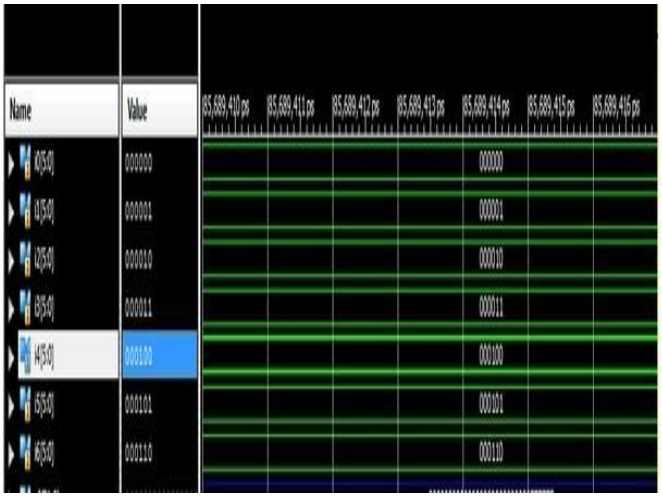

Figure 6.2 Output of FFT

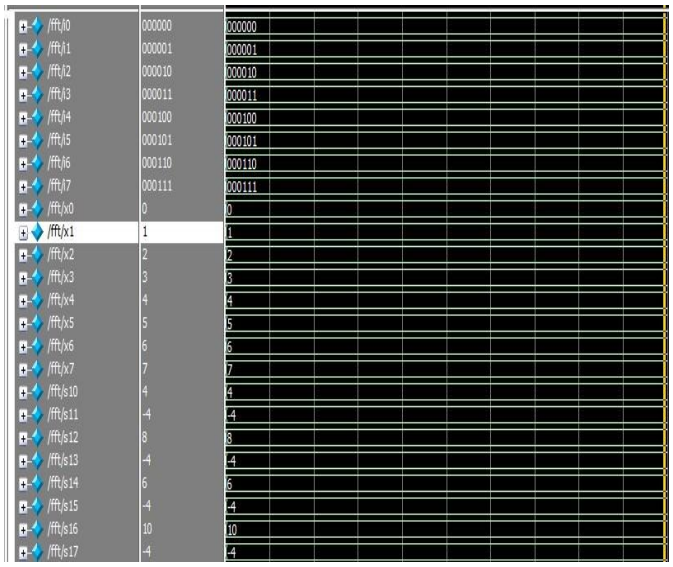

Figure 6.3 Output of FFT with CORDIC Algorithm

8. CONCLUSION

This paper has presented the Binary FFT architecture. It is the first FFT used to compute the value of output sequencs using CORDIC algorithm.It creates a data management that allows for using the theoretical minimum amount of hardware resources for a Binary FFT. Compared to previous designs, the presented Binary FFT reduces either the number of rotator, or the number of adders or the memory of the design. A solution for natural I/O has also been presented, which offers comparable results to previous natural I/O FFTs. The experimental results obtained to verify the architecture, leading to small area and low power consumption.

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